Appl. No.: 10/056,144
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APPEAL BRIEF

Mail Stop APPEAL BRIEF—PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: June 17, 2004

Sir:

Appellant hereby submits this Appeal Brief in connection with the above-identified application.

I. REAL PARTY IN INTEREST

The real party in interest is Halliburton Energy Services, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-41.
Claim cancellations:	24, 28, 32.
Added claim:	None.
Presently pending claims:	1-23, 25-27, 29-31, 33-41.
Presently appealed claims:	1-23, 25-27, 29-31, 33-41.

IV. STATUS OF THE AMENDMENTS

Applicant did not file any amendments after the final rejection.

V. SUMMARY OF THE INVENTION

A condition that interferes with optimal lithium/lithium thionyl chloride battery cell performance is excessive anode "passivation." Passivation refers to the buildup of lithium chloride ("LiCl") on the anode surface of the cell. When a load is placed on a cell having anode passivation, an initial drop in potential is observed, because the LiCl acts as a series resistor. However, as current flows through the LiCl and gradually causes the LiCl to evaporate (i.e., undergo "depassivation"), the cell potential rises. If the time period between the initial potential drop and the subsequent potential rise is substantial (e.g., as

in heavily passivated cells), the cell may be damaged. More specifically, if the cell potential drops below a predetermined minimum voltage for an extended period of time, the cell may be damaged. Applicant's Disclosure, pages 1-5.

Various embodiments of the invention are disclosed that protect a cell if the cell potential falls below a predetermined minimum voltage as described above. Figure 1 shows a cell protection circuit 50 comprising bypass device 56 coupled to a transistor 54. If the potential across cell 52 falls below a predetermined minimum voltage, the transistor 54 limits the current that flows through the cell 52 and re-directs the current around the cell 52 (i.e., through the bypass device 56), thus preserving the cell 52 from damage.

Claim 1 is directed to a cell protection circuit and is reflective of at least some embodiments of the invention. The circuit of claim 1 comprises a transistor coupled to the cell and a current bypass device coupled to the transistor and the cell. The transistor limits the current that can flow through the cell when the voltage across the cell falls to a predetermined minimum level. The current bypass device permits at least a portion of the current to bypass the cell.

VI. ISSUE(S)

1. Whether claims 1-15, 21-23, 25-27, 29-31, and 33-41 are anticipated by U.S. Patent No. 6,294,766 (*Autry et al.*).
2. Whether claims 16-20 are anticipated by U.S. Patent No. 5,600,231 (*Parker*).

VII. GROUPING OF CLAIMS

Applicant proposes the following groups of claims for purposes of this appeal:

1. Claims 1, 2 and 4 stand together (representative claim is claim 1);
2. Claim 3 stands alone;
3. Claims 5, 6, and 10 stand together (representative claim is claim 5);
4. Claims 7-9 and 11-13 stand together (representative claim is claim 7);
5. Claim 14 stands alone;
6. Claim 15 stands alone;
7. Claim 16 stands alone;
8. Claim 17 stands alone;

9. Claim 18 and 19 stand together (representative claim is claim 18);
10. Claim 20 stands alone;
11. Claims 21 and 22 stand together (representative claim is claim 21);
12. Claim 23 stands alone;
13. Claims 25, 26 and 30 stand together (representative claim is claim 25);
14. Claims 27, 29, 31 and 33 stand together (representative claim is claim 27);
15. Claim 34 stands alone;
16. Claim 35 stands alone;
17. Claims 36 and 38-40 stand together (representative claim is claim 36);
18. Claim 37 stands alone;
19. Claim 41 stands alone.

The groupings above are for purposes of this appeal only. The groupings should not be construed to mean the patentability of any of the claims can only be determined (*e.g.*, in later actions before a court) based on the groupings.

VIII. ARGUMENT

The Examiner rejected claims 1, 3, 5, 7, 14, 15, 21, 23, 25, 27, 34-38 and 41 as anticipated by Autry. The Examiner rejected claims 16-18 and 20 as anticipated by Parker. Each reference is summarized below.

A. The Parker Reference

Parker is directed to a battery testing and refreshing device. As shown in Figure 2, Parker's device includes a test circuit 22 used to determine the charge level of the battery 30 and to provide an indication of the charge level on a test display 16 (Figure 1 and column 4, lines 42-50). Parker's device also includes a refresh circuit 24 used to discharge the battery 30 to a predetermined level. Either circuit 22 or 24 can be activated by a user activating a switch (switch 12 for circuit 22 and switch 14 for circuit 24). When either circuit is activated, the battery 30 conducts current through the active circuit. That is, regardless of which circuit is active, all current flowing through the circuit also flows through the battery 30 (column 4, lines 3-15). In some situations, the zener diode 26 may prevent current from flowing through the cell 30, effectively removing the cell 30 from the

circuit (column 5, lines 20-23). However, if cell 30 is effectively removed from the circuit, then no voltage is supplied to the circuit and thus no current flows through the circuit.

B. The Autry Reference

Autry is directed to a battery protection device. Figure 1 shows a device having two discharge diodes in series, three charge diodes in series, a cell, and a solder ingot, all in parallel with one another. The solder ingot in Autry is illustrated and described as a thermally-activated (i.e., not electrically activated) "switch" comprising solder that, when heated, reflows thereby creating a short circuit (column 2, lines 4-9). Autry's circuit protects other cells in a battery pack that by creating a short circuit across the cell if the cell is failing or has failed. More specifically, if the cell fails, current is diverted from the cell and through either the charge or the discharge diodes. Autry explained that current flowing through the diodes generates heat that reflows the solder ingot (column 2, lines 35-37) and causes a short circuit across the cell. The current then flows through the short circuit and the cell is effectively removed from the battery, thus protecting other cells in the battery pack (column 1, lines 12-14).

C. The Examiner Erred In Rejecting Claim 1

The Examiner rejected claim 1 as being anticipated by Autry. For at least the reasons provided below, Autry does not teach or render obvious claim 1. Claim 1 is directed to a cell protection circuit that comprises, among other features, "a transistor coupled to said cell" and "wherein said transistor limits the current that can flow through said cell when the voltage across said cell falls to a predetermined minimum level." As explained above, Autry teaches a solder ingot that melts to form a permanent, low resistance short circuit. Autry does not teach or suggest a transistor coupled to a cell as required by claim 1. For at least this reason, Applicant respectfully submits that the Examiner erred in rejecting claim 1. For at least these same reasons, the Examiner erred in rejecting all claims that depend on or from claim 1, as well as all other claims in the same group as claim 1 (see claim grouping above).

D. The Examiner Erred In Rejecting Claim 3

The Examiner also rejected claim 3 as being anticipated by Autry. Claim 3 is directed to the cell protection circuit of claim 1 and specifies that "said transistor is

connected in series with said cell and said current bypass device is connected in parallel to said serially connected transistor and cell." Autry does not teach or even suggest this particular circuit architecture (see Autry Figs. 1 and 2). At least for this reason, and for the same reasons the Examiner erred in rejecting claim 1 on which claim 3 depends, Applicant respectfully submits that the Examiner erred in rejecting claim 3.

E. The Examiner Erred In Rejecting Claim 5

The Examiner rejected claim 5 as being anticipated by Autry. Claim 5 is directed to the cell protection circuit of claim 1 and specifies that "said transistor comprises a MOSFET." As explained above, Autry does not teach or even suggest the use of a transistor, and Autry certainly does not teach or suggest the use of a MOSFET. At least for this reason, and for the same reasons the Examiner erred in rejecting claim 1 on which claim 5 depends, Applicant submits that the Examiner erred in rejecting claim 5. For at least these same reasons, the Examiner erred in rejecting all other claims in the same group as claim 5.

F. The Examiner Erred In Rejecting Claim 7

The Examiner rejected claim 7 as being anticipated by Autry. Claim 7 is directed to the cell protection circuit of claim 6, "wherein the n-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level." As explained above, Autry does not teach the use of a transistor, nor does Autry teach or even suggest the use of a MOSFET.

The Examiner also incorrectly likened the thermally-activated solder ingot of Autry to the transistor of claim 7. The Examiner erred in this analogy because the solder ingot of Autry does not have "a threshold voltage," as required by claim 7. Furthermore, the solder ingot of Autry does not limit "the current that can flow through said cell when the voltage across said cell falls to a predetermined minimum level." At least for these reasons, and for the same reasons the Examiner erred in rejecting claim 1 on which claim 7 depends, Applicant submits that the Examiner erred in rejecting claim 7. At least for the same reasons, the Examiner erred in rejecting all claims that depend on or from claim 7, as well as all other claims in the same group as claim 7.

G. The Examiner Erred In Rejecting Claim 14

The Examiner rejected claim 14 as being anticipated by Autry. Claim 14 is directed to the cell protection circuit of claim 1 and further includes "a delay device coupled to said cell and said transistor, said delay device slows the rate of change of voltage across said cell with changes in current load on said cell." Autry does not even teach or suggest such a delay device. At least for this reason, and for the same reasons the Examiner erred in rejecting claim 1 on which claim 14 depends, Applicant submits that the Examiner erred in rejecting claim 14. At least for the same reasons, the Examiner erred in rejecting all claims that depend on or from claim 14.

H. The Examiner Erred In Rejecting Claim 15

The Examiner rejected claim 15 as being anticipated by Autry. Claim 15 is directed to the cell protection circuit of claim 14, "wherein said delay device comprises a resistor coupled to a capacitor." As explained above, Autry does not teach a delay device, and Autry certainly does not teach or suggest a delay device that comprises a resistor coupled to a capacitor. At least for this reason, and for the same reasons the Examiner erred in rejecting claim 14 on which claim 15 depends, Applicant submits that the Examiner erred in rejecting claim 15.

I. The Examiner Erred In Rejecting Claim 16

The Examiner rejected claim 16 as being anticipated by Parker. Claim 16 is directed to "a protection circuit for a cell" that comprises, among other features, "a means for limiting current through said cell when the voltage across said cell reaches a predetermined threshold." Although the Examiner correctly observes that the zener diode 26 may limit the current through the cell 30 (see Parker Fig. 2), Parker does not teach "a means for limiting current through said cell when the voltage across said cell reaches a predetermined threshold." Further, Parker does not teach or suggest "a means for bypassing current around said cell when the voltage across said cell reaches the predetermined threshold," as required by claim 16. As explained above, if the zener diode 26 prevents current from flowing through the cell 30, then the cell 30 is effectively removed from the circuit. As such, no voltage is supplied to the circuit, and current does

not flow through the cell, around the cell, or anywhere else in the circuit. Thus, Parker does not teach "a means for bypassing current around said cell." At least for this reason, Applicant submits that the Examiner erred in rejecting claim 16 and all claims that depend on claim 16.

J. The Examiner Erred In Rejecting Claim 17

The Examiner rejected claim 17 as anticipated by Parker. Claim 17 is directed to the protection circuit of claim 16, "further including a means for providing a time delay." Parker does not teach or even suggest "a means for providing a time delay." At least for these reasons, and for the same reasons the Examiner erred in rejecting claim 16 on which claim 17 depends, Applicant submits that the Examiner erred in rejecting claim 17.

K. The Examiner Erred In Rejecting Claim 18

The Examiner rejected claim 18 as anticipated by Parker. Claim 18 is directed to "a method of protecting a cell" which comprises, among other features, "when limiting the current, permitting the current to conduct through a bypass device coupled in parallel with said cell." Parker does not teach or even suggest a bypass device coupled in parallel with a cell. Further, as previously explained, the Examiner correctly observes that the zener diode 26 limits the current through the cell 30. As such, the cell 30 is effectively removed from the circuit and thus no current flows through any part of the circuit. Thus, not only does Parker fail to teach "permitting the current to conduct through a bypass device" as required by claim 18, Parker teaches the opposite. Effectively removing the cell 30 from the circuit, as taught by Parker, prevents current from flowing at all through the circuit. At least for these reasons, Applicant submits that the Examiner erred in rejecting claim 18. For at least the same reasons, the Examiner erred in rejecting all claims that fall into the same group as claim 18 as well as all claims that depend on claim 18.

L. The Examiner Erred In Rejecting Claim 20

The Examiner rejected claim 20 as being anticipated by Parker. Claim 20 is directed to the method of claim 19, "further including providing a time delay to the voltage across said transistor." Parker does not teach or even suggest implementing a time delay to the voltage across such a transistor. At least for this reason, and for the same reasons

that the Examiner erred in rejecting claim 19 on which claim 20 depends, Applicant submits that the Examiner erred in rejecting claim 20.

M. The Examiner Erred In Rejecting Claim 21

The Examiner rejected claim 21 as being anticipated by Autry. Claim 21 is directed to a battery that comprises, among other features, "a separate protection unit coupled to each cell, each protection unit protecting its associated cell." While Autry does teach a protection unit coupled to each cell, the protection unit does not protect "its associated cell," as required by claim 21. Instead, Autry clearly teaches that the protection unit protects other cells in the battery (see Autry's Abstract). Furthermore, Autry does not teach or even suggest "a transistor coupled to said associated cell," as required by claim 21. Instead, Autry teaches a thermally-activated solder ingot. At least for this reason, Applicant submits that the Examiner erred in rejecting claim 21 and all claims that fall into the same group as claim 21, as well as all claims that depend on claim 21.

N. The Examiner Erred In Rejecting Claim 23

The Examiner rejected claim 23 as anticipated by Autry. Claim 23 is directed to the battery of claim 21, "wherein said transistor is connected in series with said cell and said diode is connected in parallel to said serially connected transistor and cell." Autry does not teach or suggest the specific circuit architecture recited in claim 23. At least for these reasons, and for the reasons that the Examiner erred in rejecting claim 21 on which claim 23 depends, Applicant submits that the Examiner erred in rejecting claim 23.

O. The Examiner Erred In Rejecting Claim 25

The Examiner rejected claim 25 as anticipated by Autry. Claim 25 is directed to the battery of claim 21, "wherein said transistor comprises a MOSFET." Autry does not teach or even suggest the use of a MOSFET. At least for this reason, and for the reasons that the Examiner erred in rejecting claim 21 on which claim 25 depends, Applicant submits that the Examiner erred in rejecting claim 25. For at least these same reasons, the Examiner also erred in rejecting all the claims that fall into the same group as claim 25.

P. The Examiner Erred In Rejecting Claim 27

The Examiner rejected claim 27 as anticipated by Autry. Claim 27 is directed to the battery of claim 26, "wherein the n-channel enhancement mode MOSFET has a threshold

voltage substantially the same as the predetermined minimum level." As previously explained, Autry does not teach a MOSFET having a threshold voltage. At least for this reason, and for the reasons the Examiner erred in rejecting claim 26 on which claim 27 depends, Applicant submits that the Examiner erred in rejecting claim 27 and all claims that fall into the same group as claim 27, as well as all claims that depend on claim 27.

Q. The Examiner Erred In Rejecting Claim 34

The Examiner rejected claim 34 as anticipated by Autry. Claim 34 is directed to the battery of claim 21, "further including a delay device coupled to said cell and said transistor." Autry does not teach or even suggest the use of a delay device. At least for this reason, and for the reasons the Examiner erred in rejecting claim 21 on which claim 34 depends, Applicant submits that the Examiner erred in rejecting claim 34 and all claims that depend on claim 34.

R. The Examiner Erred In Rejecting Claim 35

The Examiner rejected claim 35 as anticipated by Autry. Claim 35 is directed to the battery of claim 34, "wherein said delay device comprises a resistor coupled to a capacitor." Autry clearly does not teach or even suggest a delay device, and certainly not a delay device that comprises a resistor and a capacitor. At least for this reason, and for the reasons the Examiner erred in rejecting claim 34 on which claim 35 depends, Applicant submits that the Examiner erred in rejecting claim 35.

S. The Examiner Erred In Rejecting Claim 36

The Examiner rejected claim 36 as anticipated by Autry. Claim 36 is directed to "a battery cell protecting circuit," "wherein the current limiter functions to limit current to the cell when the cell voltage reaches a predetermined threshold." Autry does not teach a "current limiter [that] functions to limit current to the cell when the cell voltage reaches a predetermined threshold." At least for this reason, Applicant submits that the Examiner erred in rejecting claim 36 as well as all other claims that fall into the same group as claim 36 and all claims that depend on claim 36.

T. The Examiner Erred In Rejecting Claim 37

The Examiner rejected claim 37 as anticipated by Autry. Claim 37 is directed to the circuit of claim 36, "wherein the current limiter comprises a transistor." As previously

discussed, Autry does not teach or suggest a transistor, but a thermally-activated solder ingot. At least for this reason, and for the reasons the Examiner erred in rejecting claim 36 on which claim 37 depends, Applicant respectfully submits that the Examiner erred in rejecting claim 37.

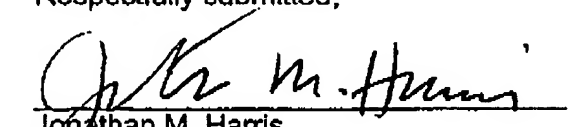
U. The Examiner Erred In Rejecting Claim 41

The Examiner rejected claim 41 as anticipated by Autry. Claim 41 is directed to the circuit of claim 36, "further including a delay element" to "delay the current limiting action of said current limiter when the cell voltage reaches the predetermined threshold." As previously discussed, Autry does not teach or even suggest a delay element. At least for these reasons, and for the same reasons that the Examiner erred in rejecting claim 36 on which claim 41 depends, Applicant submits that the Examiner erred in rejecting claim 41.

IX. CONCLUSION

Applicant respectfully requests that the rejections in the Final Office Action be reversed and the case allowed. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Conley Rose Deposit Account Number 03-2769 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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APPENDIX TO APPEAL BRIEF

CURRENT CLAIMS

1. (Previously amended) A cell protection circuit, comprising:

a transistor coupled to said cell; and

a current bypass device coupled to said transistor and said cell;

wherein said transistor limits the current that can flow through said cell when the voltage across said cell falls to a predetermined minimum level; and

wherein the current bypass device permits at least a portion of the current to bypass the cell.

2. (Original) The cell protection circuit of claim 1 wherein said current bypass device conducts current when said transistor limits the current through the cell.

3. (Original) The cell protection circuit of claim 1 wherein said transistor is connected in series with said cell and said current bypass device is connected in parallel to said serially connected transistor and cell.

4. (Original) The cell protection circuit of claim 1 wherein said current bypass device comprises a diode.

5. (Original) The cell protection circuit of claim 1 wherein said transistor comprises a MOSFET.

6. (Original) The cell protection circuit of claim 1 wherein said transistor comprises an n-channel enhancement mode MOSFET.

7. (Original) The cell protection circuit of claim 6 wherein the n-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

8. (Original) The cell protection circuit of claim 7 wherein said current bypass device comprises a diode.

9. (Original) The cell protection circuit of claim 8 wherein said n-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the negative terminal of said cell, said drain terminal couples to the anode of said diode, and the cathode of said diode and said gate terminal couple to the positive terminal of said cell.

10. (Original) The cell protection circuit of claim 1 wherein said transistor comprises an p-channel enhancement mode MOSFET.

11. (Original) The cell protection circuit of claim 10 wherein the p-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

12. (Original) The cell protection circuit of claim 11 wherein said current bypass device comprises a diode.

13. (Original) The cell protection circuit of claim 12 wherein said p-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the positive terminal of said cell, said drain terminal couples to the cathode of said diode, and the anode of said diode and said gate terminal couple to the negative terminal of said cell.

14. (Original) The cell protection circuit of claim 1 further including a delay device coupled to said cell and said transistor, said delay device slows the rate of change of voltage across said cell with changes in current load on said cell.

15. (Original) The cell protection circuit of claim 14 wherein said delay device comprises a resistor coupled to a capacitor.

16. (Previously amended) A protection circuit for a cell, comprising:

a means for limiting current through said cell when the voltage across said cell reaches a predetermined threshold; and

a means for bypassing current around said cell when the voltage across said cell reaches the predetermined threshold.

17. (Original) The protection circuit of claim 16 further including a means for providing a time delay.

18. (Previously amended) A method of protecting a cell, comprising:

limiting the current through said cell when the voltage across said cell falls to a minimum predetermined level; and

when limiting the current, permitting current to conduct through a bypass device coupled in parallel with said cell.

19. (Previously amended) The method of claim 18 wherein limiting the current through said cell is performed using a transistor.

20. (Previously amended) The method of claim 19 protecting a cell further including providing a time delay to the voltage across said transistor.

21. (Previously amended) A battery, comprising:

a plurality of cells connected in series; and

a separate protection unit coupled to each cell, each protection unit protecting its associated cell and comprising:

a transistor coupled to said associated cell; and

a diode coupled in parallel with said transistor and said associated cell to cause current to be automatically diverted from said cell when a voltage meeting or exceeding a threshold voltage of the diode is applied to said diode;

wherein said transistor limits the current that can flow through said associated cell when the voltage across said associated cell falls to a predetermined minimum level.

22. (Previously amended) The battery of claim 21 wherein said diode conducts current when said transistor limits the current through the cell.

23. (Previously amended) The battery of claim 21 wherein said transistor is connected in series with said cell and said diode is connected in parallel to said serially connected transistor and cell.

24. (Canceled).

25. (Original) The battery of claim 21 wherein said transistor comprises a MOSFET.

26. (Original) The battery of claim 21 wherein said transistor comprises an n-channel enhancement mode MOSFET.

27. (Original) The battery of claim 26 wherein the n-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

28. (Canceled).

29. (Previously amended) The battery of claim 27 wherein said n-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the negative terminal of said cell, said drain terminal couples to the anode of said diode, and the cathode of said diode and said gate terminal couple to the positive terminal of said cell.

30. (Original) The battery of claim 21 wherein said transistor comprises an p-channel enhancement mode MOSFET.

31. (Original) The battery of claim 30 wherein the p-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

32. (Canceled).

33. (Currently amended) The battery of claim 31 wherein said p-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the positive terminal of said cell, said drain terminal couples to the cathode of said diode, and the anode of said diode and said gate terminal couple to the negative terminal of said cell.

34. (Original) The battery of claim 21 further including a delay device coupled to said cell and said transistor, said delay device slows the rate of change of voltage across said cell with changes in current load on said cell.

35. (Original) The battery of claim 34 wherein said delay device comprises a resistor coupled to a capacitor.

36. (Previously amended) A battery cell protection circuit, comprising:

a current limiter capable of being coupled to a battery cell; and

a bypass device coupled in parallel with the current limiter and cell, said bypass device adapted to direct current flow around said cell;

wherein the current limiter functions to limit current to the cell when the cell voltage reaches a predetermined threshold.

37. (Original) The circuit of claim 36 wherein the current limiter comprises a transistor.

38. (Original) The circuit of claim 36 wherein the current limiter comprises an n-channel MOSFET.

39. (Original) The circuit of claim 36 wherein the current limiter comprises a p-channel MOSFET.

40. (Original) The circuit of claim 36 wherein said bypass device comprises a diode.

41. (Original) The circuit of claim 36 further including a delay element coupled to said current limiter to delay the current limiting action of said current limiter when the cell voltage reaches the predetermined threshold.